REMARKS

Applicants thank the Examiner for the continued detailed examination of the present application as evidenced by the Final Official Action dated February 27, 2003 (herein after the "Final Official Action). Although, Applicants maintain that the claims as written are patentable over Sato, independent Claim 35 has been amended to further clarify the subject matter recited therein. Also, Applicants have cancelled Claims 40-42 in an effort to advance prosecution of the present application and to narrow the issues for continued prosecution of the application and/or appeal.

Applicants submit that no new issues are raised by this amendment as the recitations of independent Claim 35 have only been further clarified and have not been narrowed in view of Sato. Furthermore, rejected Claim 42 has been cancelled without prejudice or disclaimer. Accordingly, Applicants respectfully request entry of the present amendment after final and the allowance of Claims 35, 36, and 38, and 39, which remain pending upon entry of the present amendment.

For the sake of brevity, Applicants' remarks herein focus on the recitations of amended independent Claim 35 and the comments on Applicants' previous response. However, to ensure that the present amendment after final is fully responsive to the Final Official Action, all of Applicants' previous responses are hereby incorporated herein by reference in their entireties.

The rejection under section 112 is now moot.

Claim 42 is rejected under 35 USC § 112. *Final Official Action, page 2.* As discussed above, Claim 42 has been cancelled without prejudice or disclaimer. Accordingly, the rejection of this claim is now moot.

Amended independent Claim 35 is patentable over Sato.

Claims 35, 36 and 38-42 stand rejected under 35 USC § 102 over U.S. Patent No. 5,739,587 to Sato ("Sato"). *Official Action, page 5.* Independent Claim 35 has been amended to recite in-part:

forming a dielectric layer on an integrated circuit substrate;
forming a via hole in the dielectric layer to expose the substrate;
and
forming a conductive pattern in the via hole and on the dielectric layer to form a closed via through the dielectric layer to the substrate to enclose an inner portion of the dielectric layer within the closed via that is separated from an outer portion of the dielectric layer that is outside the closed via.

As understood by Applicants, Sato does not disclose all of the recitations of amended independent Claim 35. For example, Sato does not disclose "**forming a conductive pattern in the via hole... to form a closed via through the dielectric layer to the substrate to enclose an inner portion of the dielectric layer within the closed via that is separated from an outer portion of the dielectric layer that is outside the closed via**." It appears from the Final Official Action, that the Examiner considers elements 102/45 to disclose the above cited recitations, however, as understood by Applicants, elements102 and 45 in Sato are actually alternative embodiments which are mutually exclusive (*Final Official Action, page 3*). In particular, FIGs. 4 and 8 show, respectively, that element 45 is a solid type via whereas element 102 is a conductor in a groove that surrounds a through-hole via as discussed at *Sato, col. 6, lines 36-40*. As understood by Applicants, these elements are, therefore, incompatible with one another as element 45 cannot enclose another element, which appear to be required by element 102. Therefore, Sato does not disclose "forming a conductive pattern in the via hole... **to form a closed via through the dielectric layer to the substrate to enclose an inner portion of the dielectric layer within the closed via that is separated from an outer portion of the dielectric layer that is outside the closed via**" as recited in amended independent Claim 35.

With regard to the comments on Applicants' arguments in the previous response, Applicants respectfully point out that the detailed analysis provided by Applicants actually discussed Figures 3, 8, and 11, and was not limited to Figures 1 and 3 as stated in the Final Official Action. *(See the Final Official Action, page 6).*

In particular, Applicants' arguments regarding Sato in the previous response were as follows:

> In an effort to further clarify Applicant's reasoning and to advance prosecution of the present application, Applicant provides herein a detailed analysis of Figures 3, 8 and 11 and the associated passages of Sato cited by the Official Action.
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> As understood by Applicant, Figure 3 of Sato illustrates an interlayer insulation film 60 having a plurality of interlayer connection conductors 40-45. The interlayer connection conductors 40-45 appear to have the same structure as that of conductor 120 shown in Figures 1 and 2 of Sato (see, for example, the passage in Sato relating to the diameters of the interlayer connection conductors). *Sato, column 5, lines 5-8.*
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> In contrast to Figure 3 of Sato, independent Claims 35 and 40 recite, in-part, "forming a dielectric layer . . . including a closed via therein . . . that encloses an inner portion of the dielectric layer and is enclosed by an outer portion of the dielectric layer." As illustrated by Figures 1, 2 and 3 of Sato, the conductors that pass through the dielectric layer, appear to be solid, cylindrical structures that do not enclose **any** portion of the interlayer insulation film 60 (alleged to disclose the dielectric layer recited in the claims). Accordingly, Figures 1-3 of Sato do not disclose all of the recitations of independent Claim 35 as required under section 102.
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> As understood by Applicant, Figure 8 of Sato is a plan view of an upper electrode layer 100 including a center through-hole. Furthermore, Figure 8 illustrates concentric structures 102 and 103 around the center through-hole in the upper electrode layer 100. The conductors 102 and 103 shown in Figure 8 are **grooves** in the upper electrode layer, and do not appear to pass through the upper electrode layer into what would be an interlayer insulation film (as illustrated, for example, in Figure 3 of Sato). For example, the relevant portion of Sato states that As shown in FIG. 8, furthermore, **grooves may be formed in concentric circles around a through hole. Conductors 102, 103 and 104 may be embedded into the grooves and through hole.** The double-groove layout can reliably prevent the moisture from entering the semiconductor device. *Sato, col. 6, lines 36 to40.*
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> As understood by Applicant, a groove does not disclose a hole. The above-cited passage of Sato demonstrates that Figure 8 illustrates a through hole (having a conductor 104) in the upper electrode layer 100 and concentric grooves that have conductors 102 and 103 embedded therein.

Moreover, even assuming for the sake of argument that the conductors 102 and 103 shown in Figure 8 did pass through the upper electrode layer 100, such a structure would still not disclose all the recitations of independent Claims 35 and 40. In particular, independent Claims 35 and 40 recite in-part that the closed via (included in the dielectric layer) "extends from the first face to the second face" (of the dielectric layer). In contrast to Figure 8 of Sato, in some embodiments according to the present invention as illustrated, for example, in Figure 2 of the application, the interdielectric layer pattern 48b has first and second opposing faces (bordering, for example, layers 46a and 50a, respectfully). The interdielectric layer pattern 48b includes a closed via which is illustrated in the cross-section of Figure 2 by the sections labeled as S2. In the plan view of Figure 1, the areas S2 are shown as being part of a closed via 54 that encloses an inner portion of the interdielectric layer pattern 48b and is enclosed by an outer portion of the interdielectric layer pattern 48a. Furthermore, the closed via in the interdielectric layer pattern 48b (as illustrated by portions as S2 in Figure 2) extends from the first face of the interdielectric layer pattern 48b to the second face of the interdielectric layer pattern 48b. Accordingly, Figure 8 of Sato also does not disclose the recitations of independent Claim 35 as required under section 102.

As understood by Applicant, Figure 11 of Sato illustrates a structure (similar to the structure shown in Figure 3) but with an additional interlayer insulation film 540 having holes therein and conductors 611 that pass through the holes to contact a bottom electrode layer 550. *See, for example, Sato, column 7, lines 1-11.* Sato, therefore, appears to add only another layer of the same structure shown in Figure 3 of Sato which, as discussed above, also does not disclose the recitations of independent Claims 35 and 40. Accordingly, Figure 11 also does not disclose all of the recitations of independent Claim 35 as required under section 102.

As shown above, Applicants' analysis did show, in detail, why Sato does not disclose all of the recitations of the claims as required under section 102. Moreover, Applicants respectfully maintain that all of the arguments are on-point regarding why Sato does not meet the requirements of a rejection under section 102. Accordingly, Applicants respectfully request entry of the present amendment and the allowance of all claims in due course. If any informal matters arise, the Examiner is invited to contact the undersigned by telephone at (919)854-1400.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF; Commissioner for Patents, Washington, DC 20231, on April 28, 2003.

Audra Wooten
Date of Signature: April 28, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Sir:

The following is an addendum to the concurrently filed amendment in response to the final Official Action dated February 27, 2003 in the above referenced application. This addendum includes a marked-up version of the changes made to the claims by the present amendment.

In the Claims:

Claim 35 has been amended as follows:

35. (Twice Amended) A method of forming a bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer [having first and second opposing faces] on an integrated circuit substrate[, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer];

forming a via hole in the dielectric layer to expose the substrate; and

forming a conductive pattern in the via hole and on the dielectric layer to form a closed via through the dielectric layer to the substrate to enclose an inner portion of the dielectric layer within the closed via that is separated from an outer portion of the dielectric layer that is outside the closed via [that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate].

Claims 40-42 have been cancelled without prejudice or disclaimer.

END